REMARKS

Claims 1-8, 10-12, 14-23, and 25-27 are presented for examination. Claims 1, 10, 23, and 26 are currently amended. Claims 9, 13, and 24 have previously been canceled. No new claims have been added.

In the Office Action Claims 1-5, 7-8, 23, and 25 were rejected under 35 USC § 102(e) as being anticipated by Hong et al., U.S. 6,933,755 ("Hong"). Claims 6, 10-12, 14-22, and 26-27 were rejected under 35 USC 103(a) as being unpatentable over Hong.

Hong

Claims 1, 10, 23, and 26 are currently amended. Support for the amendments can be found in the specification as filed, for example, at paragraphs [0047] and [0053], and Figures 1A, 1B, 1C, and 1D.

Hong teaches, as is typical of the prior art, level shifters (100', 110') separate from delay compensating unit (320). Hong teaches transmission gate TG1 for equalizing timing at the level shifters (col. 5, lines 57-60 and col. 7, lines 15-20; Fig. 3). Hong teaches transmission gate TG2 for equalizing timing in the delay compensating unit (col. 7, lines 30-39; Fig. 3). Also, for example, at Figure 3, Hong is silent with regard to break before make operation and teaches equal timing at the output of the delay compensating unit (320) (col. 7, lines 30-40, and Fig. 3). Further, for example, at Figure 4, Hong teaches equal timing using INV18 and TG4 at the output signal generating unit 440 (col. 8, lines 56-62; col. 8, line 63 through col. 9, line 4, and Figs. 4 and 5). Hong then teaches using the equal timing to pulse the driving transistors PM6 and NM 6 momentarily while using a latch (441) comprising INV19 and INV20 to sustain the output current to the load (col. 8, lines 10-22, Figs. 4 and Figs. 5H, 5I, and 5J). Applicants agree with the Office action that "Hong does not expressly state the size value for the transistors" and thus may be assumed to be equal in Hong.

Contrary to teaching adjusting the size of transistors to affect circuit timing as in the present invention, Hong teaches providing additional circuit elements (e.g., transmission gates TG1 through TG4, Figs. 3,4) for compensating for delays of various corresponding inverters (e.g., inverters INV6, INV9, INV11, INV 18, respectively) and teaches making the delays ***equal*** (col.7, lines 15-45) rather than ***unequal*** and thus teaches away from the present invention's use of size as in amended claim 1 where: "the first NFET is larger than the second PFET, creating unequal delays between the output of the first inverter falling to logic zero and the output of the second inverter rising to logic one" and "the second NFET is larger than the first PFET, creating unequal delays between the output of the second inverter falling to logic zero and the output of the first inverter rising to logic one" so that delays in the sense of Hong are unequal.

Likewise, Hong teaches equal transistor sizes and equal delays that equalize circuit timing. Therefore, each of the outputs of Hong's cross coupled inverters must rise ***at the same time*** that the other falls, not ***before*** as in amended claim 10, in which

> "the NFETs of the cross-coupled inverters are larger than the PFETs of the cross-coupled inverters, said NFETs and PFETs being sized with respect to each other such that:
>
> each of the first and second outputs of the two cross-coupled inverters falls to logic zero before the other of the first and second outputs rises to logic one in response to a transition in the input signal"

and as in amended claim 26, in which

> "sizing the NFETs and PFETs of the cross-coupled inverters such that each of the NFETs are larger than each of the PFETs of the cross-coupled inverters so that a first time constant to charge a first output of the cross-coupled inverters is greater than a second time constant to discharge a second output so that the second output discharges before the first output charges; and so that a third time constant to charge the second output of the cross-coupled inverters is greater than a fourth time constant to discharge the first output so that the first output discharges before the second output charges"

Therefore, the structure and principles of operation of the present invention claimed by amended claims 10 and 26 are contrary to those disclosed by Hong.

Because Hong teaches equal transistor sizes and equal delays to equalize circuit timing, each of the outputs of Hong's cross coupled inverters must charge ***at the same time*** that the other discharges so that there is ***no delay*** between either of the outputs charging relative to the other output discharging, contrary to amended claim 23 in which

> "the cross-coupled inverter means includes first and second outputs, the first output has a first delay charging relative to the second output discharging, the second output has a second delay charging relative to the first output discharging, and said first and second delays are created by the unequal transistor sizes of the cross-coupled inverters;
>
> first and second output buffer means for receiving the first and second outputs of the cross-coupled inverter means, for inverting the first output of the cross-coupled inverter means while leaving the second output of the cross-coupled inverter means uninverted so that the first output buffer means provides a break transition before the second output buffer means provides a make transition due to the second delay, and the second output buffer means provides a break transition before the first output buffer means provides a make transition due to the first delay".

Therefore, Applicants respectfully submit that Hong neither anticipates nor makes obvious the present invention as claimed by the amended claims 1, 10, 23, and 26 and that the section 102 and 103 rejections should be withdrawn.

Conclusion

In light of the arguments and amendments presented herein, the Applicants respectfully submit that all pending claims are in condition for allowance. Accordingly, reconsideration and allowance of this Application is earnestly solicited. Should any issues remain unresolved, the Examiner is encouraged to telephone the undersigned at the number provided below.

Respectfully submitted,

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